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09/697305

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**U.S. UTILITY Patent Application**

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PATENT DATE

TR. 3K(B) Q.A. LP  
SCANNED

APPLICATION NO.	CONT/PRIOR	CLASS 111	SUBCLASS 33	ART UNIT	EXAMINER
09/697305	F	324 AS	265 AS	2858 9133	METTAHIE

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R59

# Fault detecting method and layout method for semiconductor integrated circuit

PTO-2040  
12/99

**ISSUING CLASSIFICATION**

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
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